

A Verification Methodology for OPP

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Abstract

Electronic system-level (ESL) design is emerging as a technique for managing the exponential growth in the complexity of system hardware and software. However, system-level modeling requires a verification methodology that is both efficient and thorough. The methodology must be able to trace a failure to the design component responsible for it, so that it can be corrected. The verification environment must exercise each component sufficiently within the context of the system model to minimize the chance of a fault going undetected. Both the tests and the verification code written for such an environment should be reusable at several levels of design abstraction. The environment should also allow design requirements to be represented in an unambiguous form and compared easily with the actual behavior of the design. We present a methodology based on abstract forms of boundary scan and assertions, which we believe can meet all of the above needs. The methodology is implemented in C++ and SystemC, providing maximum flexibility for the coding of tests and testbenches and facilitating integration with high-level design environments.